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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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WOLF GREENFIELD & SACKS, PC
FEDERAL RESERVE PLAZA
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,996	HOMEWOOD ET AL.	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3 – 9, 13 – 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Lewis et al (U.S. Patent No. 5,797,043 hereinafter "Lewis").

3. As to Claims 1 and 24, Lewis teaches a system comprising:

a processor for executing instructions; (Host Processor, element 12, figure 1a)

a stream register unit connected to supply a first type of data to the processor, the first type of data being data supplied from a peripheral (I/O Channel Controller, element 62, figure 3, element 140, figure 5a);

a FIFO connected to receive said first type of data from the peripheral (FIFO Pool Bus, column 14, lines 25 – 29) and connected to the stream register unit by a communication path, along which said first type of data can be supplied from the FIFO to the stream register unit (FIFO pool subsystem, figure 6); and

a memory bus connected between a data memory and the processor, across which the processor can access the second type of data, the second type of data being

randomly accessible data held in the data memory (Processor Bus, element 16', figure 2).

4. As to claim 3, Lewis teaches a system, wherein data is supplied from the FIFO to the stream register unit accordance with requests for data made (requested function, column 13, 23 – 30) by the processor to the stream register unit and forwarded to the FIFO (FIFO pool buffering functions, column 12, lines 38 –58).

5. As to claim 4, Lewis teaches a system, wherein the said requests are made as accesses to volatile variables (10 Bit – Request variable changes consistently per requested lines of data and can be changed at any time, Table VIII).

6. As to claim 5, Lewis teaches a system wherein the FIFO is arranged to, upon receiving a request for data from the stream register unit, send a signal to the stream register unit indication availability of the requested data (available space and data, Table VII sent via BTU, element 170 figure 5b.).

7. As to claim 6, Lewis teaches a system, wherein if the FIFO contains the requested data, the said signal to the stream register unit indicates that the data is available, and the FIFO is further arranged to send (burst data transfer, column 20, lines 1 – 4) a signal (transfer signals, Table VI) to the stream register unit comprising the data (column 19, lines 64 – 67, column 20, lines 1 – 35).

8. As to claim 7, Lewis teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, supply the data (data stream, element 76, figure 3) to the processor (column 10, lines 25 – 41, passed to DSP, column 20 lines 5 - 35).

9. As to claim 8, Lewis teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, send a signal to the FIFO indicating that it has taken the data (Transfer Done, Table VII).

10. As to claim 9, Lewis teaches a system, wherein the said signal to the FIFO further indicates the next location in the FIFO from which the data is required (next sequential, column 16, lines 10 – 33).

11. As to claims 13 and 25, Lewis teaches a system, further comprising a timeout generator, arranged for communication with the processor and the stream register unit, and arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available (data available in the FIFO, Table VIII), after a predetermined period of time, send a timeout signal to the processor, causing the processor to interrupt (Interrupt, Table III & XXIV) such that it can execute other instructions (column 36, lines 1 – 17).

12. As to claim 14, Lewis teaches a system, wherein if following sending of the timeout signal to the processor the data subsequently becomes available, the timeout generator is arranged to receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal (column 36, lines 18 – 40).

13. As to claim 15, Lewis teaches a system, wherein the stream register unit is arranged to, if following sending of the timeout signal to the processor the data subsequently becomes available, send the data to the processor (in response to host interrupts, the host processor provides for the transfer of data, column 26, lines 25 – 34).

14. As to claim 16, Lewis teaches a system, wherein the stream register unit is associated with a register file containing a plurality of registers (register based interface, column 22, lines 15 – 33) and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 19, lines 52 – 63).

15. As to claim 17, Lewis teaches a system, wherein the processor is arranged to retrieve data from the register file (column 22, lines 15 – 33).

16. As to claim 18, Lewis teaches a system, wherein data is supplied from the FIFO to the stream register unit in accordance with requests for data made by the processor

to the stream register unit and forwarded to the FIFO (figure 1a and 1b), wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 19, lines 52 – 63), wherein the processor is further arranged to make requests for data to the stream register unit via the load/store unit (column 33, lines 33 – 39).

17. As to claim 19, Lewis teaches a system, wherein the stream register unit comprises one or more FIFOs connected to receive data from the FIFO connected to the stream register and supply the data to the processor (FIFO 0 – 3, elements 210 – 212, figure 5c).

18. As to claim 20, Lewis teaches a system, wherein the request for data is a request for a single data item (column 10, lines 30 - 41).

19. As to claim 21, Lewis teaches a system, further comprising one or more additional FIFOs linked (FIFO 0 – 3, elements 210 – 212, figure 5c) together between the said FIFO and the communication channel (FIFO pool subsystem, figure 6).

20. As to claim 22, Lewis teaches a system, wherein the data from the peripheral is video data (video words, column 25, lines 37 – 40).

21. As to claim 23, Lewis teaches a system, wherein the peripheral is a video processing system (video controller, column 25, lines 29 – 48).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of George et al. (US Patent Number 6,785,829, hereinafter "George").

24. As to claim 2, Lewis teaches a system, comprising a processor for executing instructions; and a stream register unit connected to supply data from the peripheral to the processor.

Lewis fails to teach a system wherein the stream register unit forms part of the processor.

George teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of George.

One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to efficiently optimize a system with regards to real estate in compactness and means of high-speed processing.

25. Claims 10 thru 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of Lai et al. (US Patent Number 6,433,785 hereinafter "Lai").

26. As to claim 10, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

Lewis fails to teach system wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available.

Lai teaches a system, wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available (first defer identifier, column 3, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Lai. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to optimize a request process in which resources are valuable and delays need to be minimized, improving processor to device throughput.

27. As to claim 11, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

Lewis fails to teach system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions.

Lai teaches a system, wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions (issue a stop signal, column 3, lines 20 - 26).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Lai. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system.

28. As to claim 12, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

Lewis fails to teach system wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit.

Lai teaches a system, wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit (when the initiator is ready, data transfer between the initiator and the responder begins, column 3, lines 32 – 34).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Lai. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system requesting data.

29. Claim 26 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of Garcia et al. (US Patent Number 6,433,785 hereinafter "Garcia").

30. As per claims 26 and 30, Lewis teaches a stream register connectable between a processor and peripheral and between a processor and a memory, comprising:

a receiver arranged to receive a request for a data item from the processor (column 10, lines 30 - 41); and

a stream engine (element 76, figure 3), arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item (I/O Channel Controller, element 62, figure 3),

and, if the data item is available (available space and data, Table VII sent via BTU, element 170 figure 5b.), send the data item to the processor.

Lewis fails to teach a register wherein if the data item being requested is not available, sending a timeout signal to the processor.

Garcia teaches a register wherein if the data item being requested is not available, sending a timeout signal to the processor (timeout counter, column 5, lines 26 – 42)

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Garcia. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to optimize a request process in which resources are valuable and delays need to be minimized, improving processor to device throughput.

31. As to claim 27, Lewis teaches a stream register, wherein the stream engine is arranged to the interrupt signal to the processor after a predetermined period of time (Interrupt, table III).

32. As to claim 28, Lewis teaches a stream register, wherein the stream engine is further arranged to, if the data is available, temporarily store the data in a register file for access by the processor (temporarily stored in a FIFO within the bus master units, column 19, lines 52 – 63).

33. Lewis modified by the teachings of Garcia as applied to claims 26 and 30 above, in regards to claim 29, Lewis teaches a stream register, wherein the stream engine is further arranged to temporarily store (column 19, lines 52 – 63) the data in a register file for access by the processor (column 18, lines 29 – 36).

Lewis fails to teach a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, if the data item subsequently becomes available, receive a signal instructing it to cease sending the timeout signal, and to upon receipt of the said instruction cease sending the timeout signal to the processor.

Garcia teaches a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, if the data item subsequently becomes available (posted write buffer available signal 350, column 5, lines 30 – 31), receive a signal instructing it to cease sending the timeout signal, and to upon receipt of the said instruction cease sending the timeout signal to the processor (column 5, lines 26 – 42).

Response to Arguments

The Examiner respectfully acknowledges the Applicant's arguments and explanations, as they have deemed helpful in understanding the specification of the current application.

34. Applicant's arguments filed 8/9/2006 have been fully considered but they are not persuasive. The Applicant argues:

1.) Lewis does not teach or suggest that two separate types of data can be supplied to a processor, first type being data supplied directly from a peripheral and a second type of data being directly randomly accessible data held in a data memory.

2.) Lewis does not teach supplying data to the processor via the stream register unit in the received order.

3.) Lewis is silent on sending a stall signal or timeout signal to a processor if a data item is not available from a peripheral and Garcia teaches a write buffer in a memory controller is not available when a processor is attempting to write information to a graphics device, excluding the motivation to combine Lewis and Garcia.

35. As per argument 1, the Examiner respectfully disagrees. The Applicant has provided ample basis and explanation to better understand the specification however the arguments do not completely pertain to claim limitations. The claim limitations define a first and second type of data and accordingly via the system are supplied to the processor. Nowhere in the claim limitations is citation of direct supply of data from the peripheral to the processor. Instead there is a stipulation that the type of data is supplied via a stream register unit. The Examiner has cited the stream register unit to be the I/O controller and accordingly the data streaming is handled therein. Hence data of the first type via the stream register unit, whether or not a memory is involved as that is not in the claim limitations, is supplied at the discretion of the I/O controller to the

processor as seen in figure 2. The second type of data is interpreted as any data that resides in the memory and is interfaced to the processor via a memory bus. As seen in figures 1a and 2 the processor has access to the type of data defined as second according to the claim limitations. Also the processor in Lewis has the ability to control all peripherals accessible via a bus as seen in figure 1b, column 15, lines 18 – 24. There is no exclusivity of where the data resides, the only limitations set forth in the claims are that the stream register unit supplies a first type of data and the processor has the ability to randomly access the second type of data. Clearly from this explanation and citation one of ordinary skill in the art would realize that the claim limitations teach no exclusivity and that Lewis completely fulfills the required first and second types of data as connectively defined in claim 1.

36. As per argument 2, the Examiner respectfully disagrees. In light of the explanation cited above and the interpretation of claim limitations the Examiner refers to figure 1b in which the processor via the stream register unit and FIFO and bus has direct control over all peripherals connected therein. In a system where data is streamed directly it would follow that the term direct would be best interpreted as a consecutive order that in turn translates to received order of data. Clearly from this citation one of ordinary skill in the art one would realize that direct control attributes to a consecutive nature, hence data is supplied to the processor in the order in which it was received by the stream register unit.

37. As per argument 3, the Examiner respectfully disagrees. The Examiner asserts that the functionality of a timeout or stall signal with respect to the current application and current prior art of the record is in the scope of, as cited in the 1st Office Action, to optimize a process where resources are valuable and delays need to be minimized improving the processor to device throughput. The Examiner further expresses that in a system dealing with an I/O Controller and digital signal processor the availability of resources as in this case said peripherals is a critical element to efficiency. Whether reading or writing from and to a peripheral is a different matter. The Examiner was motivated to combined Garcia with Lewis in order to assert the optimizing characteristics of a timeout and stall when a peripheral is not available. The matter of whether it is a read/write process is not the purpose of Garcia. The purpose is solely for handling a peripheral when not available to a system. From this clarification of what essential elements were required of Garcia one of ordinary skill in the art would realize that a timeout and stall signal is indeed essential to a resource intense system of Lewis and such characteristics are appropriately found in Garcia.

Conclusion

38. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH

KIM HUYNH
SUPERVISORY PATENT EXAMINER
10/30/06